

Philips Semiconductors





Abstract

This application note deals with the smart card interface TDA8002. It explains how to handle I^2C cards with this interface.

APPLICATION NOTE

USING I2C CARDS WITH THE TDA8002

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> Keywords TDA8002 Smart Cards I²C protocol

Date : November 1996

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1. Introduction

Due to the internal IO line configuration, it is not possible to communicate with standard I^2C cards using only IO as SDA line.

This document gives two hardware methods to solve this problem by separating the I/O input and output on the host side :

- the first method uses IO_uC as output and AUX2_uC (or AUX1_uC) as input,

- the second method uses IO_uC as output and a standard microcontroller port of the host plus a gate as input.

This second method should be implemented if the auxiliary outputs are already used to drive C4 and C8 contacts of other synchronous cards.

This report is written for the version C2 of the TDA8002, where CLK and STROBE have the same polarity.

2. TDA8002 problem description

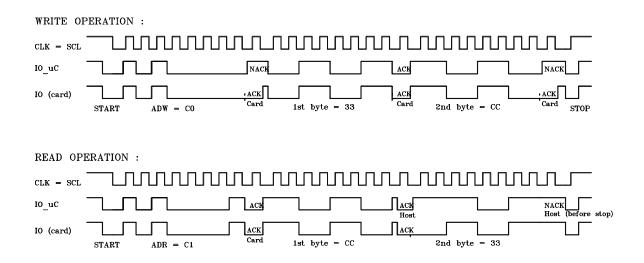
The TDA8002 I/O line is a false bi-directionnal line with IO pin on card side and IO_uC pin on host side. It is defined in the specification as follows :

« the first side on which a falling edge is detected becomes a master (input). An anti-latch circuitry first disables the detection of the falling edge on the other side, which becomes slave (output) ».

So, the I/O line can not switch from transmission configuration to reception without a falling edge. That is not compatible with I^2C specification where, during a communication (between start and stop conditions), the default level on SDA may be the low level and where the bit ACK set by the receiver may leave SDA at a low level.

The problem occurs in transmission to the card if the host sets the SDA line high for receiving the ACK bit after the card has set the SDA line low for transmitting the ACK bit ... Then, the SDA line is never high and there is no high to low transition enabling the receiver to become transmitter.

The same problem happens in reception from the card after the ACK bit has been sent by the host : if the host sets the SDA line high to receive the next byte after the card has prepared its first bit to low (if the byte is smaller than 80 H), there is no high to low transition and the first bits are lost until the card sets the SDA line high then low.

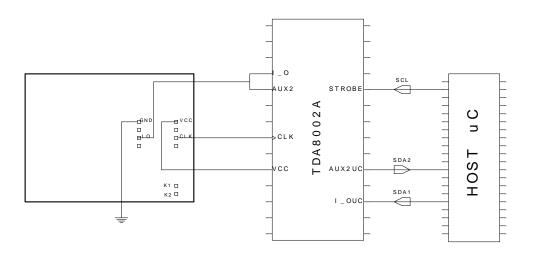


3. First solution : use of IO and AUX

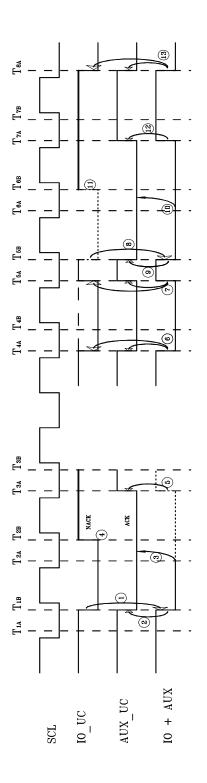
The first solution proposed is to use two lines for handling the card SDA : IO and AUX2 (or AUX1 if AUX2 is not available). AUX2 has been chosen in this example because IO and AUX2 are physically close to each other and AUX1 may be used to drive the C4 contact of some synchronous cards. On the card side, IO and AUX2 should be linked and on the system side, IO_uC is used as output (SDA1) and AUX2_uC is used as input (SDA2).

The I²C clock SCL is transferred on the CLK pin of the card through the STROBE input of the TDA8002.

This solution is available if the microcontroller input is in high impedance state at high level. If it is not the case, it may be necessary to add an open collector gate (7407 type) between the TDA8002 AUX output and the microcontroller input.



Explanation :



Case A		data from host to card ACK from card to host		
a-	IO falls	ets the last data bit at 0 low IC copys the low level of IO	at T _{1B}	1 2
b-	(IO_uC	l sets IO low for ACK bit is still a 0) 1C copys the ACK	at T _{2A}	3
	if IO_uC	C is set high by the software eceive the ACK bit), it stays in emission	at T_{2B} mode	4
C-		let IO high to be in reception mode aC goes high and IO_uC is still in emission	at T _{3A}	5
At T _{3B} ,	IO may v	write its first data bit to 1 or 0.		
Case B		data from card to host ACK from host to card		
IO_uC	is set higl	n during the reception mode		
a-		l sets its last data bit to 0 nC copys the low level	at T _{4A}	6
b-		sets IO high for the reception of ACK aC and IO_uC go high	at T _{5A}	7
C-	IO falls	s set low for ACK low aC copys IO low	at T _{5B}	8 9
d-		l sets the first data bit at 0 on IO aC stays at 0 during this bit	at T _{6A}	10
e-		high for reception but emission mode until next low level 3)	at T _{6B}	11

In this diagram, the microcontroller IOs are bi-directionnal, and are put in reception by beeing set high (8051 IO types). If it is not the case, IO_uC may stay in emission mode, but it must be set high during the read operations.

In this configuration, and almost during the read operation it is important that the microcontroller always sets its level on IO_uC at T_{nB} (low level for ACK) after the card has set the IO line at T_{nA} (high during host ACK). The solution is to set the IO_uC bit just before setting SCL high, because the card always sets its IO bit on the falling edge of SCL and reads the bit on the rising edge.

Example :

The following routines give an example of use with a 80C51 microcontroller. A complete example software and its schematic are given in annex 1.

start:	setb setb call clr call clr	SDA1	;generation of a start condition
; iicwbyt	 ۵۰		;routine for writing 1 byte
newbyt	setb	с	;acknow bit
	mov	r7,#9	;8 bits + acknow
byte_lo			,
• –	rlc	а	
	mov nop	SDA1,c	;write the bit
	setb	SCL	
	call	wait6	
	clr	SCL	
	djnz	r7,byte_loop	

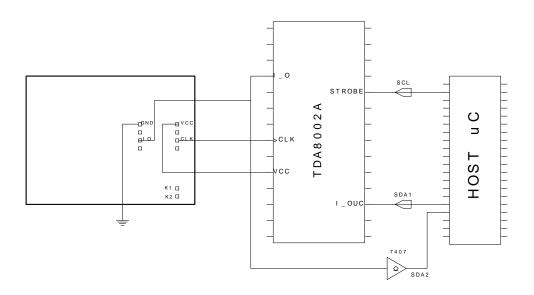
;			
iicrbyte:			;read one byte and send ACK
	clr	c	;acknow bit
iicr_na	ck_byte:		;(read one byte and send NACK)
	mov	a,#0ffh	
	mov	r7,#9	;8 bits + acknow
byte_lo	-		
	rlc	a	
	nop		
	nop		
		SCL	
	call		
		c,SDA2	;read the bit
	clr		
	djnz	7,byte_loop	
; stop:			;generation of a stop condition
I	clr	SDA1	
	setb	SCL	
	call	wait6	
	setb	SDA1	
	setb	SDA2	
,			
wait6:			
	nop		
	nop		
•			
wait4:			
wait4:	ret		

4. Second solution : use of IO and one microcontroller port

This second solution is also the use of two lines for driving the card SDA, but only one goes through the TDA8002, the IO line which is used as output, the second line beeing directly derived from the host microcontroller and used as input.

In order to be sure that this second line is always in a high impedance state, a 7407 gate (non inverter, open collector output) is put between the host port and the IO pin.

The two lines are linked on the card I/O pin.



The driving software is the same as above.

This solution requires to protect the 7407 gate against ESD up to 6 kV while the first solution does not require any external component because the AUX1 or AUX2 lines have the same level of ESD protection as I/O.

ANNEX

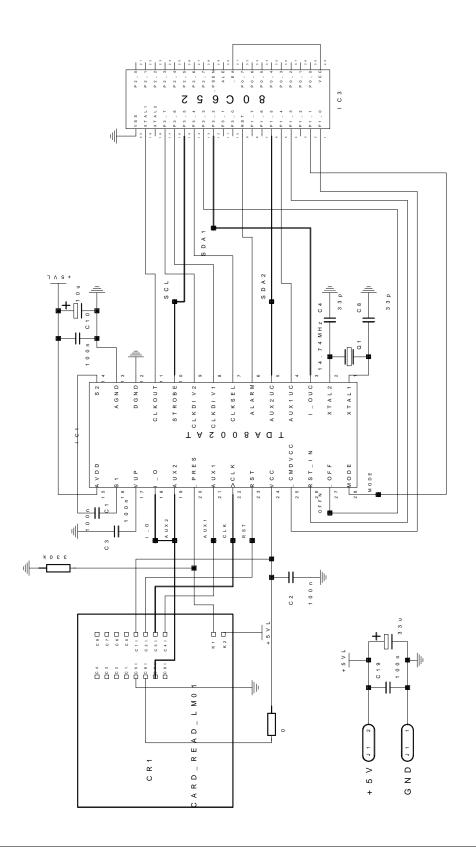
Example using AUX2 and IO

This example is a standard application of the TDA8002 driving asynchronous and synchronous smart cards where the C8 contact is not connected.

Only the routines for driving I^2C cards are given here, with a very simple application layer written for the Philips D2000 card:

- read 4 bytes at current address
- write FF, FE, FD, FC at address 0
- read 4 bytes at address 04.

The case of a non acknowledge is not handled.



SDA2 : p1.5 SDA1 : p3.2 SCL : p3.5	= = =	AUX2_uC of TDA8002 IO_uC of TDA8002 STROBE of TDA8002
adw = 0a0h adr = 0a1h		;i ² c write address (D2000 card) ;i ² c read address
nbroct: 1 byte	=	number of data to read or write (including memory address if needed)
stadd: 1 byte	=	start address of the data buffer
addbuf: 1 byte	=	card memory address buffer
datbuf: 8 bytes		data buffer

;* datbuf must be placed just after addbuf in RAM

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Master I<sup>2</sup>C
•
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; - Start condition sub-routine

; - The iicbyte routine write the data on

; SDA1 on a low level of SCL and read the

; data on SDA2 on the high level of SCL :

; - the data to send must be in the Acc,

; and the read data is available in Acc.

; - To read, Acc must be first set to FFh.

; - ACK bit is available in the carry.

; - The ACK error routine depends on the

; application, and is not handled here.

SDA2

SCL

SDA1 wait6

start:

;generation of a start condition ;AUX2 is used as input

clr SDA1 call wait6 SCL

setb

setb setb

call

clr

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iicwby	vte: setb	с	;routine for writing or reading one byte ;acknow bit
iicbyte			
	mov	r7,#9	;8 bits + acknow
byte_l			,
2 —	rlc	а	
	mov	SDA1,c	;write the bit
	nop		
	setb	SCL	
	call	wait4	
	mov	c,SDA2	;read the bit
	clr	SCL	
	djnz	r7,byte_loop	
	ret		
;			
iicrbyt	e:		;read one byte and send ACK
•	clr	с	;acknow bit
iicr_l_			;(read one byte and send NACK)
	mov	a,#0ffh	
	jmp	iicbyte	
;			
stop:			;generation of a stop condition
stop.	clr	SDA1	generation of a stop contained
	setb	SCL	
	call	wait6	
	setb	SDA1	
	setb	SDA2	
;			

wait6:			
wallo.	nop		
	nop		
wait4:	-		
	ret		
·***** '	******	******	****
write_i	ic:		
	mov	r0,stadd	;data buffer base address
	mov	r1,nbroct	;number of data to transmit
	mov	a,#adw	;write address
	call	start	;start condition + write address
	jc	ack_erro	:
	J		,
write_l	oop:		
	mov	a,@r0	
	call	iicwbyte	
	jc	ack_error	
	inc	r0	;increment data address
	djnz	r1,write_loop	;decrement data counter
	ret		
•*****		****	****
,	*****	*****	****
;***** read_ii	******* C:		
,	******** c: mov	r0,stadd	;data buffer base address
,	******* c: mov mov	r0,stadd r1,nbroct	;data buffer base address ;number of data to receive
,	******** c: mov	r0,stadd	;data buffer base address
,	******* c: mov mov	r0,stadd r1,nbroct	;data buffer base address ;number of data to receive
,	******* c: mov mov mov	r0,stadd r1,nbroct a,#adr	;data buffer base address ;number of data to receive ;read address
, read_ii	******** mov mov call jc	r0,stadd r1,nbroct a,#adr start	;data buffer base address ;number of data to receive ;read address
,	******** mov mov call jc	r0,stadd r1,nbroct a,#adr start ack_error	;data buffer base address ;number of data to receive ;read address
, read_ii	******** c: mov mov call jc cop: djnz	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes	;data buffer base address ;number of data to receive ;read address
, read_ii	******** mov mov call jc	r0,stadd r1,nbroct a,#adr start ack_error	;data buffer base address ;number of data to receive ;read address
, read_ii	******** c: mov mov call jc cop: djnz jmp	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes	;data buffer base address ;number of data to receive ;read address
, read_ii read_lo	******** c: mov mov call jc cop: djnz jmp	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes	;data buffer base address ;number of data to receive ;read address
, read_ii read_lo	********* c: mov mov call jc oop: djnz jmp ytes: call mov	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes read_last iicrbyte @r0,a	;data buffer base address ;number of data to receive ;read address ;start condition + read address
, read_ii read_lo	********* c: mov mov call jc call jc djnz jmp ytes: call	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes read_last iicrbyte @r0,a r0	;data buffer base address ;number of data to receive ;read address ;start condition + read address
, read_ii read_lo	********* c: mov mov call jc oop: djnz jmp ytes: call mov	r0,stadd r1,nbroct a,#adr start ack_error r1,read_bytes read_last iicrbyte @r0,a	;data buffer base address ;number of data to receive ;read address ;start condition + read address

read_last: setb с iicr_l_byte ;read the last byte and send a NACK call @r0,a mov ret ;----ack_error: nop ret ; Initialisation of the TDA8002 ; for the I2C communication ****** init: r0,#0ffh mov clr а clr_ram: mov @r0,a djnz r0,clr_ram init_tda8002: setb mode setb clksel ;AUX_ μ C and IO_ μ C must be set high before activation SDA1 setb setb SDA2 SCL setb ;activation of the VCC reset_card: clr cmdvccn r2,#250 mov

wait_ac	ctiv:		
	djnz	r2,\$	
	call	seq1	
	call	seq2	
	call	seq3	
end:	jmp	end	
;			
seq1:	mov mov call call ret	r0,#datbuf stadd,r0 nbroct,#5 read_iic stop	;read 4 bytes at current address
;			
seq2:			;write FF FE FD FC at address 0
	mov mov	r0,#addbuf stadd,r0	
	mov	nbroct,#5	;address + 4 bytes
	mov	addbuf,#0	;Card memory address
	mov	r0,#datbuf	
	mov	r1,#0ffh r2,#4	
s2_wlo	mov op:	12,#4	
5	mov	a,r1	
	mov	@r0,a	;write FF FE FD FC in datbuf
	inc	rO	
	dec	r1	
	djnz	r2,s2_wloop	

;-----

seq3	mov mov mov call	r0,#addbuf stadd,r0 nbroct,#1 addbuf,#4 write_iic	;read 4 bytes at address 4 ;card memory address
	mov mov call call ret	r0,#datbuf stadd,r0 nbroct,#4 read_iic stop	